REMARKS

The Office Action mailed May 31, 2002 has been reviewed and the comments of the Patent and Trademark Office have been considered. Claims 1-31 were pending in the application, with claims 12-14, 22 and 24 being withdrawn from consideration. Claims 1, 4, 11, and 23 are amended, no claims have been cancelled or newly added. Therefore, claims 1-31 are pending in the application, with claims 1-11, 15-21, 23 and 25-31 submitted for reconsideration. Entry and reconsideration based on the instant amendment and reply is respectfully requested because it is believed to place the application in condition for allowance or at the very least reduce the number of issues in an appeal.

In the Office Action, claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent 5,583,059 to Burghartz (hereafter "Burghartz"). Claims 5-11 and 15-31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Burghartz as applied to claims 1-4 above and further in view of U.S. patent 5,241,214 to Herbots et al. (hereafter "Herbots"). Applicants respectfully traverse these rejections for at least the following reasons.

First, amended independent claims 1, 4, 11, and 23 recite, *inter alia*, that the first region (including at least a first group IV element) and the second region (including the first group IV element) and formed on the first region, are of an identical conductivity type. This recited structure is not disclosed or suggested by any of the applied references. Specifically, Burghartz describes that n-collector layer 4 (Si), p-SiGe base layer 5 (SiGe) and n-emitter region 6 (Si) are subject to epitaxial growth in a bipolar transistor for a Bi-CMOS device. In constrast, the gate electrode recited in these claims has n-Si, n-SiGe and n-Si layers (or p-Si, p-SiGe and p-Si layer, or n-SiGe or n-Si layers) structure. That is, Burghatz does not disclose or suggest the explicitly recited structure in these claims nor their specific advantages that are discussed in the specification. See, for example, pages 30-31 in the specification for some of the advantages provided by the claimed structure.

Furthermore, pending claim 15 already recited that the above features but the Office Action did not address this recited feature. Specifically, the Office Action on page 4 refers to same reasons for rejections as per earlier pending claims 1-3. However, the additional

features recited in claim 15 were not addressed in the Office Action. Specifically, Burghartz does not disclose or teach the claimed structure, for example, of a semiconductor region Si/SiGe/Si and that each layer has the same conductivity type. Furthermore, Burghartz does not describe or suggest shallowing the source and drain that is facilitated by the claimed invention. Accordingly, the rejection of claim 15 is erroneous and should be withdrawn. Therefore, pending independent claim 15 and the amended independent claims 1, 4, 11, and 23 are patentable over the relied-upon references.

Second, the Office Action states that Burghatz allegedly discloses or suggests that its Bipolar transistor may be extended to BiCMOS with respect to the claimed invention. See page 5 of the Office Action. However, Burghartz describes, at col. 6, lines 30-34, that both the FET regions are masked during the epitaxial growth wherein the mask is opened only over the bipolar device site. In other words, Burghartz shows that the band gap of the bipolar transistor is narrowed by Ge, but does not teach or suggest applying this structure to an FET. Accordingly, the relevant teachings in Burghatz relates only to a bipolar transistor rather than a FET with respect to the application to Bi-CMOS. Furthermore, neither leakage of B nor prevention of variations of threshold voltage due to insufficient diffusion of As can be accomplished by Burghartz. Accordingly, this provides an additional patentable difference between the claimed invention and the relied-upon prior art.

Independent claim 28 is also believed to be allowable for some of the same reasons that have been discussed above. Specifically, claim 28 recites, *inter alia*, an elevated gate electrode formed on the main electrode wherein both of the electrodes have the same conductivity. The elevated electrode includes a third region, having a third group IV element and a fourth group IV element, in contact with the main electrode, and a fourth region formed in contact with the third region and including the third group IV element. These and other recited features of claim 28 are also not taught or suggested by the relied upon prior art. Accordingly, claims 28 is believed to be patentable over the applied prior art.

The dependent claims are also patentable for at least the same reasons as the independent claims on which they ultimately depend. In addition, they recite additional patentable features when considered as a whole.

In view of the foregoing, applicants believe that the application is in condition for allowance and entry and reconsideration is respectfully requested If there are any questions regarding the application or if an examiner's amendment would facilitate the allowance of one or more of the claims, the examiner is invited to contact the undersigned attorney at the local telephone number below.

A petition with fee for a one month extension of time is enclosed.

Respectfully submitted,

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September 30, 2002
Date

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Attached: Attachment A

Should additional fees be necessary in connection with the filing of this paper, or if a petition for extension of time is required for timely acceptance of same, the Commissioner is hereby authorized to charge deposit account No. 19-0741 for any such fees; and applicants hereby petition for any needed extension of time.

ATTACHMENT A

Marked up version of claim amendments made in the Amendment filed September 30, 2002

1. (Three Times Amended) A semiconductor device comprising:

a pair of main electrodes used as source and drain electrodes;

an insulating gate film adjacent to the pair of main electrodes; and

a gate electrode comprising of a first region including at least a first group IV element and a second group IV element and formed in contact with the insulating gate film, and a second region including the first group IV element and formed on the first region, the first region and the second region having an identical conductivity type.

4. (Three Times Amended) A semiconductor device comprising:

an insulated gate field effect transistor comprising a pair of main electrodes used as [a] source and drain electrodes, an insulating gate film adjacent to the pair of main electrodes, and a gate electrode comprising a first region including at least a first group IV element and a second group IV element and formed in contact with the insulating gate film, and a second region including the first group IV element and formed on the first region, the first region and the second region having an identical conductivity type; and

a silicide electrode formed in contact with the second region of the gate electrode, and being substantially free from the second group IV element.

11. (Three Times Amended) A semiconductor device comprising:

an insulated gate field effect transistor having a pair of main electrodes used as source and drain electrodes, an insulating gate film adjacent to the pair of main electrodes, and a gate electrode comprising a first region including at least a first group IV element and a second group IV element and formed in contact with the insulating gate film, and a second region including a multiple element compound including at least the first and second group IV elements and metal, and formed on the first region, the first region and the second region having an identical conductivity type; and

a silicide electrode formed in contact with the second region of the gate electrode, including the first group IV element and metal, and being substantially free from the second group IV element.

23. (Three Times Amended) A semiconductor device comprising:

an insulated gate field effect transistor having a pair of main electrodes used as source and drain electrodes, an insulating gate film adjacent to the pair of main electrodes, and a gate electrode comprising a first region including at least a first group IV element and a second group IV element and formed in contact with the insulating gate film, and a second region including the first group IV element and formed on the first region, the first region and the second region having an identical conductivity type;

a respective elevated electrode formed on the main electrodes, and having a third region including a third group IV element and a fourth group IV element and a fourth region formed on the third region and including the third group IV element;

a first silicide electrode formed in contact with the second region of the gate electrode, and being substantially free from the second group IV element; and

a second silicide electrode formed in contact with the fourth region of the elevated electrode, and being substantially free from the fourth group IV element.